EFFICIENT ACTIVE CLAMP FOR OFF-LINE APPLICATIONS USING L4990 and L6380.

by

N.TRICOMI, C.ADRAGNA, G.GATTAVARI

SGS-THOMSON Microelectronics, Via C.Olivetti 2, 20041- Agrate Brianza,Italy

ABSTRACT

By using in kit two new standard integrated circuits, a fast PWM controller and a high voltage level shifter, it is possible to realize all the necessary control functions for an efficient and low cost off-line switching power supply with active snubber. Considering the possibility to apply the active snubber network to different topologies, a forward converter is analyzed here.
The active snubber recovers energies generated by magnetizing current and leakage inductance; core DC flux is also reduced, and the voltage breakdown requirement on the power switching element is minimized over a wide range of input supply voltages. By using the magnetizing and leakage inductance energies, we are able to turn on the power switching element with minimum drain voltage, minimizing the switching losses too.
The benefits of this approach, for autoranging applications, with duty cycle higher than 50% are also taken into account. A comparative table of results, referred to a switching frequency of 200kHz and 300kHz, when using active snubber and standard RCD snubber is given; the considered maximum output power is above 120W.

INTRODUCTION

In isolated power converters, flyback or forward, a single switch solution is the preferred choice because it allows an easy power MOS gate drive (source grounded), a higher switching frequency, and finally is low cost. Unfortunately this solution requires circuits such as clamps and snubbers to reduce the voltage peak and the switching losses on the power element. The peak drain voltage is due to the transformer leakage inductance while the switching losses depend on the turn-on capacitive energy and on the rise and fall time of the current. Moreover, in forward converters the recirculation of the magnetizing current has to be taken into account too. Traditional solutions such as a tertiary winding introduce more structural complexity on the transformer and RCD clamp reduces efficiency. This paper describes and analyzes a simple circuit realizing all the well known advantages of an active clamp.

SYSTEM DESCRIPTION

The system core uses two new integrated circuits , the L4990, advanced PWM controller, and the L6380, high voltage level shifter. While the PWM controller is realized in BCDII, the high voltage level shifter is realized in BCD off-line, with a guaranteed breakdown voltage of 600V.
Fig.1a,b) show the two devices: Fig. 1a) is related to the L4990, Fig. 1b) to the L6380, and Fig.1c) shows the L6380 die layout.

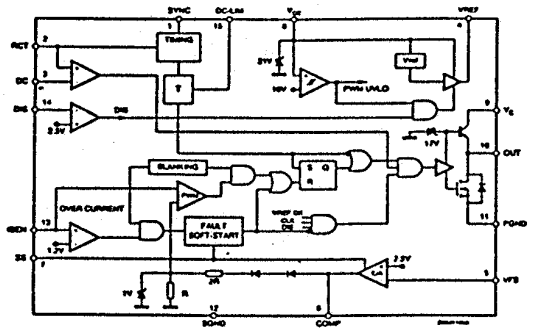

Fig.1a) L4990, PWM controller block diagram.

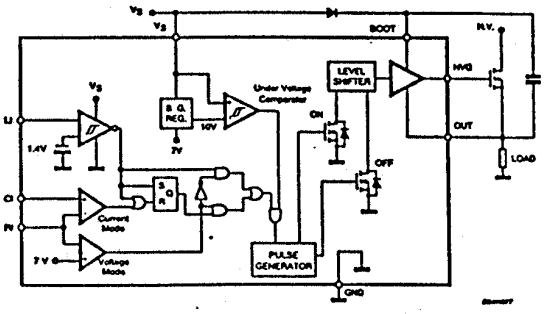

Fig.1b) L6380, level-shifter block diagram.

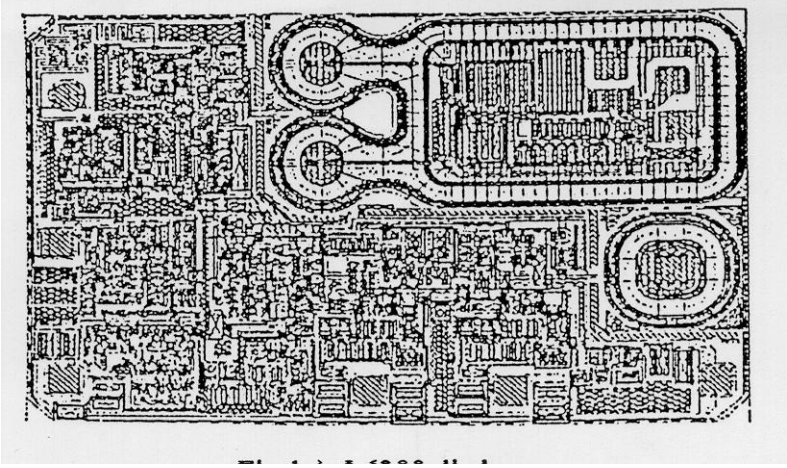

Fig.1c) L6380 die layout

The L4990 block diagram of Fig. 1a) shows a single-ended current mode controller, with all the principal blocks for a complete control functionality. The device has been designed for high frequency operation, well above the 300kHz selected for the application here described, a precise 5V +/- 2% reference voltage is externally available.
Fig. 1 b) shows the architecture of the L6380, off-line level shifter, while Fig. 1c) shows the peculiarity of the high voltage floating pocket. The architecture of this device consists of a floating gate driver, up to 600V, with a current capability, of 300mA peak source and 500mA peak sink.
An input for a logic signal, LI, is available and two additional inputs, CI and RI, connected to two internal comparators, originally designed to provide on-board current control, ground compatible, give the device enough flexibility to be employed in different types of applications.

Particular care has been taken in designing the two high voltage transistors and the relative driving logic, to provide an efficient low-loss signal level shifting. Fig. 2 shows the simplified schematic diagram of the active clamp.

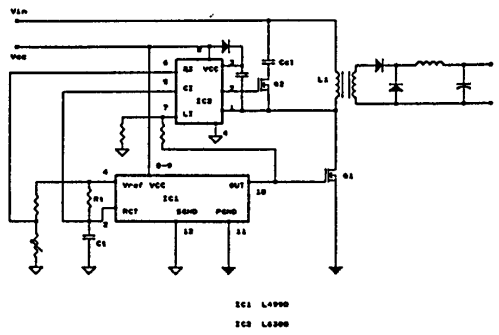

Figure 2:
Active clamp basic schematic

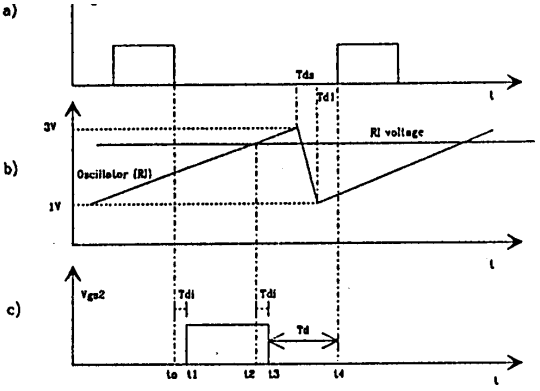

Figure 3:
System waveforms.

LI input, active low, has been connected to the output of the PWM controller, obtaining the correct phase between the driving signals of the external transistors, Q1 and Q2.
Connecting CI to the PWM oscillator pin, and RI to a voltage divider coming from the PWM controller reference voltage, also the potentially dangerous cross-conduction between the two transistors has been eliminated. Fig. 3 shows the most significant waveforms. Fig. 3 a) shows the Vgs1, gate-source voltage of Q1, generated by the PWM controller. Fig. 3b) shows the oscillator waveform of the PWM controller and the dc voltage value, lower than the peak of the oscillator waveform, at pin RI of the level shifter device. Fig 3 c) shows the Vgs2, gate to source voltage of the Q2 transistor.
Starting the sequence description of the waveforms from to, point at which Q1 is turned off, Q2 is turned on after a delay time, Tdi, estimated in about 300ns, that is the internal propagation delay of this signal in the L6380. At the beginning of Q2 conduction, the magnetizing and leakage inductance energies are transferred into the clamp capacitor, Ccl. A first resonant cycle between the primary of the transformer and the clamp capacitor starts. When the oscillator voltage, applied to CI pin (non-inverting input) reaches the threshold voltage set at pin RI (inverting input) at time t2, Vgs2 goes down turning off Q2, after the same internal propagation delay of about 300ns.
After that, starts a second resonance cycle, between the primary inductance and the Coss and layout stray capacitances. After t3, the oscillator reaches the peak value and starts the discharge ramp time down to 1V, in about 220ns(Tds) when using 1nF for Ct. Reached the valley value of the oscillator, Q1 is turned on in the following period after the 100ns of internal propagation delay, Td1, of the PWM controller.

The relationship between the RI threshold voltage and the requested delay time,Td, is:

$$V_{RI}=3-\frac{2}{T-Td_s}*(Td+Tdi-Td1-Tds) \qquad (1)$$

where T is the period of the selected switching frequency. All the parameters are in ns.
To have a Vdss at turn-on of Q1 as low as possible, the Td delay time should approach one quarter of the period of the second resonance cycle. Fig 4 is a graphical representation of equation (1), for three different operating switching frequencies.

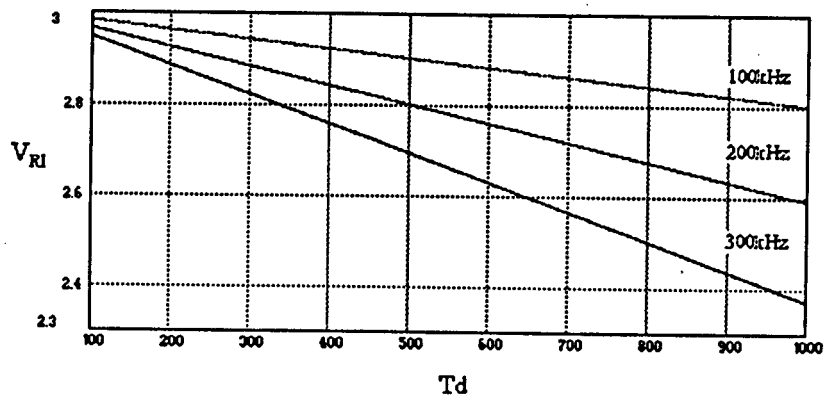

Figure 4: RI voltage vs Td delay time (Ct=1nF)

The L6380 has a 1V hysteretic UVLO, with a maximum turn-on threshold of 11V and a minimum turn-off threshold of 9V. The L4990 has a 6V hysteretic UVLO, with a minimum turn-on threshold of 15V. This is the optimum situation to guarantee the correct start-up sequences, very important to avoid core saturation.
High dv/dt latch-up immunity is requested for this application, and the level shifter we have used can withstand at least 50V/ns; DIP8 and SO8 packages are available for both the assembly possibilities.

APPLICATION DESCRIPTION

As a test vehicle to demonstrate the advantages of the active clamp, a forward converter single transistor has been chosen, with the following electrical specification:

Input voltage : 220VAC +/- 20% (110VAC manually selectable)
Output power : 150W max.
Outputs : 5V-20A, 12V-4A
Switching frequency : 300kHz

A single power MOS switch with a Vdss of 800V has been employed. The transformer is an ETD39 with low loss 3F3 core material, particularly suited for high frequency operation.
Fig. 5 shows the schematic diagram of the complete application.
For more details on the complete PWM and level shifter devices, to calculate static and dynamic power supply parameters, please refer to the literature.
The standard solution for recovering the magnetizing current consists of an additional winding, with the number of turns calculated according to the breakdown capability of the power elements or the maximum used duty cycle; this tertiary winding has to be wound to minimize the leakage inductance. An ultrafast high voltage diode must be used, and the recirculation of the magnetizing current through the input capacitor produces additional EMI/RFI noise.

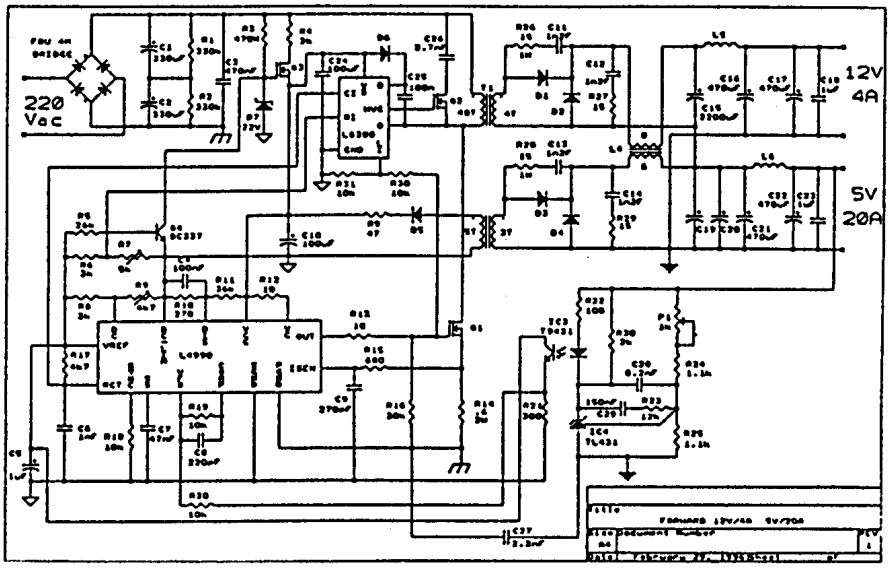

Figure 5: Forward application

A passive RCD network is the possible standard alternative to the tertiary winding technique, that sometime forces the use of a bigger core size, worsening the coupling with the secondary winding too. It is possible to have maximum duty cycles higher than 50%, particularly convenient in autoranging applications, paying for a higher BVdss. Additional power losses have to be considered when using this voltage clamping technique. The power losses on the clamp resistor depend on the values of the leakage inductance and the magnetizing current. The magnetizing energy, after defined the transformer parameters, is a constant value while the leakage energy depends on the peak primary current squared.
For the above reason, a low transformer leakage inductance is required; for having this result, a special care should be taken in choosing the appropriate core geometry, applying at the same time the appropriate winding technique.
The active clamp solves at the same time the problems generated by the introduction of the tertiary winding, the additional power dissipation and criticality in using the RCD clamping technique. At the MOS turn-off, the active clamp allows to store the leakage inductance energy, to recirculate the magnetizing current into the clamp capacitance and to use this energy for the reset of the core. When the transformer current is reduced to zero, the clamp capacitor charge forces a reverse current on the primary, with Q2 still on. At the beginning of this new situation the reverse current starts to flow into the primary of the transformer, recharging the primary inductance. After a programmed delay time, Q2 is turned off and the current into the inductance, that cannot change instantaneously, is sustained by the power MOS Coss.

Coss is starting to be discharged. The Vdss is decreasing till the power MOS is turned on again; reduced turn-on Vdss means lower parasitic switching losses.
Moreover, at turn-on time, the hysteresis core cycle is in the third quadrant; this is turning into the benefit to work far away from the saturation core point, or by using the same mechanical core, a higher power can be transferred to the secondary side.
If it is the case of need for reducing the voltage stress on Q2, when a higher voltage mains is available for the application, or it is just convenient to reduce the voltage breakdown for cost reasons, a modified schematic diagram is suggested in Fig. 6.
Now two caps in series are required, with half breakdown voltage, and the additional diode is necessary for recharging the bootstrap capacitor.

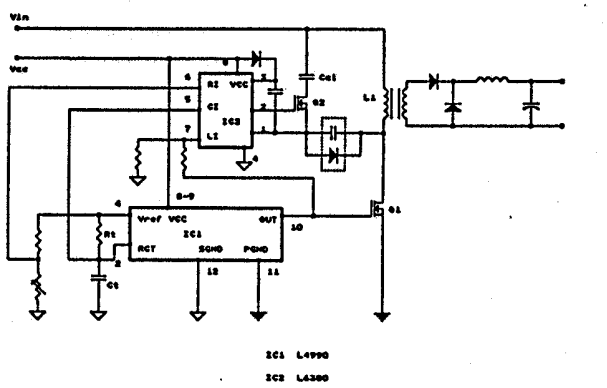

Figure 6: Modified active clamp

This scheme introduces the advantage of decoupling the level shifter parasitic capacitance, using the Coss only for the resonance. This benefit is evident in Fig. 7, where it is possible to see that the same power MOS turns on with lower Vdss.

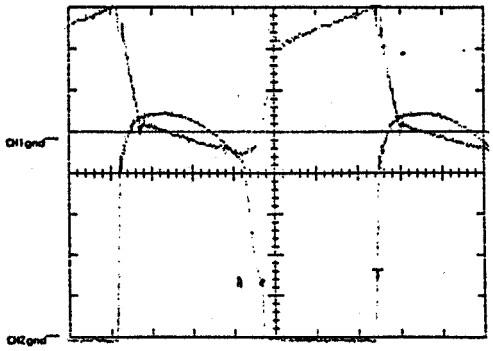

Figure 7: Primary current and drain voltage of modified active clamp
CH1:0.5A/div CH2: 100V/div Time: 500ns/div

This figure represents the current flowing into the primary of the transformer and the power MOS drain voltage, for an input voltage of 260VDC, a switching frequency of 300kHz, with an output power of 120W.
When active clamp is used, minimization of the leakage inductance is no longer vital for the application because this energy is shifted between two reactive elements, and not dissipated in heat. The active clamp can also be properly used when a planar transformer is requested.

Clamp capacitance design procedure (Fig 2)

The first step is to define the reset clamping voltage as a function of the maximum operating duty cycle, by using the below equation:

$$V_{res} = \frac{Virumax \cdot Dmax}{1-Dmax} \qquad (2)$$

where Vinmin is the minimum DC input voltage (for a 220VAC mains, 200VDC is considered, and for 110VAC, 100VDC is considered). This allows us to define the maximum voltage across the capacitor, as a function of the maximum operating duty cycle (the maximum duty cycle influences the RMS drain current). The second step is to define the maximum drain voltage, by using the following equation:

$$Vds = Vi + \frac{Vinmin \bullet Dmax}{1 - \frac{Virumin \cdot Dmax}{Vi}} \qquad (3)$$

where Vi is the maximum input DC voltage, equal to 370V.

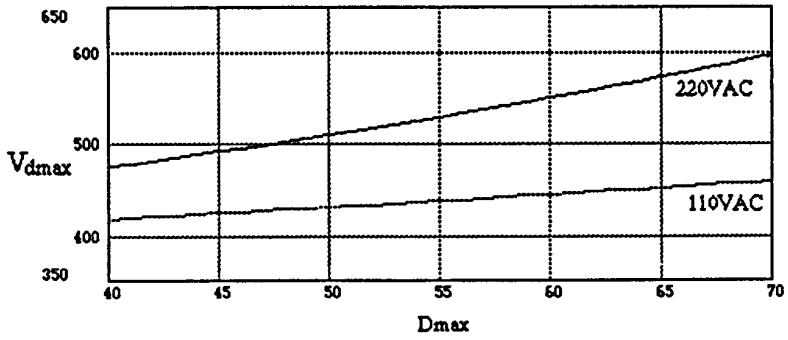

Figure 8: Maximum drain voltage vs max.duty cycle for 110VAC (autoranging) and 220VAC

Moreover, in addition to the Vds calculated with the formula (3), the clamp capacitance ripple voltage has to be considered too. This equation is represented in Fig. 8 as a function of Dmax.
This figure shows that a maximum duty cycle of 65% is practically usable, maintaining a margin of about 50V lower to the maximum rating voltage of the level shifter. This maximum duty cycle can be fixed by using the DC pin, maximum duty cycle control, pin3 of the PWM controller. Equations (2) and (3) are valid for a clamp capacitor ripple voltage negligible with respect to Q1 Vdss.

The third step is now to choose the correct clamp capacitor value in order to satisfy the above condition. Equation (4) helps in calculating the capacitor value:

$$DV_{clamp} = I_{to} \cdot \sqrt{\frac{L}{C}} \cdot tg\left[\frac{1}{4 \cdot \sqrt{L \cdot C}} \cdot \left(1 - \frac{Vinmax \cdot Dmax}{Vi}\right)\right] \qquad (4)$$

where Ito is intended the equivalent current flowing on the primary inductance, at time to of Fig3. Its value is calculated by using equation (5):

$$I_{to} = \sqrt{\left(\frac{Im}{2}\right)^2 + \frac{L_{lk}}{L} \cdot I_{pk}^2 - \frac{Coss}{L}(V\,ds)^2} \qquad (5)$$

where:

L	is the primary inductance (1.7 mH, 0.1mm air gap)
Llk	the leakage inductance (0.03 mH)
C	the clamp capacitance
Coss	the output MOS capacitance
Im	the magnetizing current with active clamp
Ipk	the peak primary current

The results are shown in Fig. 9, for an output power of 100W, with two operating switching frequencies of 200kHz and 300kHz. A 0.1mm air gap has been introduced to maximize the active clamp performance. The gap decreases the primary inductance value, increasing the resonance frequency between L and Coss, reducing, the discharge time of Coss.

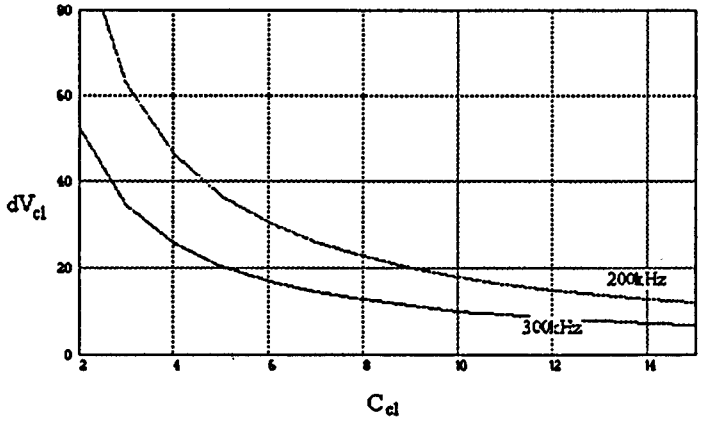

Figure 9: Ripple voltage vs clamp capacitance in full load condition and maximum input voltage

In our demo we chose a capacitor clamp of 2.7nF that produces a maximum ripple voltage of 40V at 300kHz and 60V at 200kHz. When choosing the clamp capacitor value, the requirements on dynamic performance of the power supply have to be taken into consideration too. An excessively large capacitor value decreases the ripple voltage, but it can compromise the line and load transients. Our choice criterion was to select a capacitor that produces a ripple voltage of 20% of the Vdss calculated with formula (3).

EXPERIMENTAL RESULTS

A 150W off-line forward converter has been designed and realized, for demonstrating the benefits in introducing an active clamp technique. A commercial transformer has been employed, with consumer type winding technique, oriented to minimize the cost and not the leakage inductance. Here below are listed the lab measurements.
Figs 10 show the efficiency comparison between RCD, active clamp and active clamp with improved performance with additional air gap in the transformer. For all the working measurement conditions and different clamp topologies, a maximum 45% of duty cycle has been considered; the Vdss maximum has been limited to 600V, when maximum mains and full load.

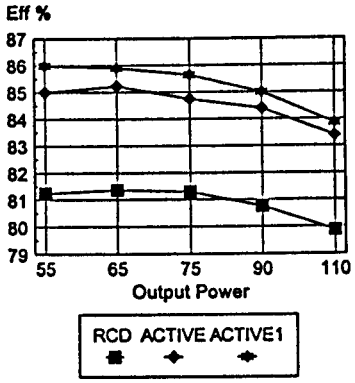

Fig.10a) Efficiency versus output power 200kHz-240Vdc

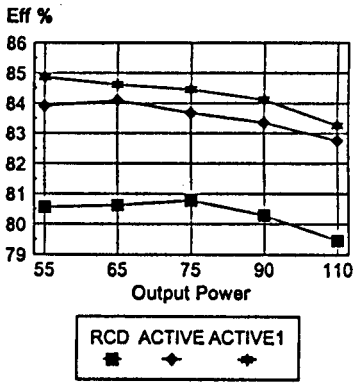

Fig.10b) Efficiency versus output power 200kHz-330Vdc

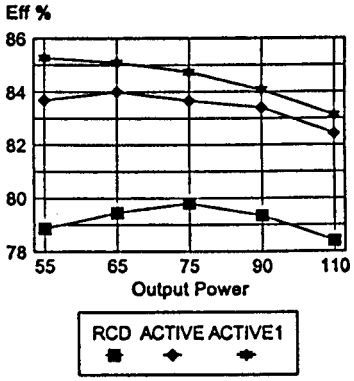

Fig.10c) Efficiency versus output power 300kHz-240Vdc

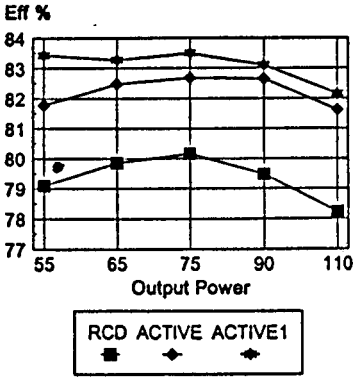

Fig.10d) Efficiency versus output power 300kHz-330Vdc

This extensive efficiency comparison between RCD and active clamps, shows an average of 3% improvement with standard active clamp approach, and up to 4% for active clamp modified by adding a 0.1mm airgap on the transformer.

Fig.11 show the basic voltage and current waveforms, related to the solution using a 0.1 mm air gap; output power is 100W and dc supply voltage is 350V. Without any airgap, the peak current due to leakage inductance, and the negative slope of the magnetizing current are reduced.

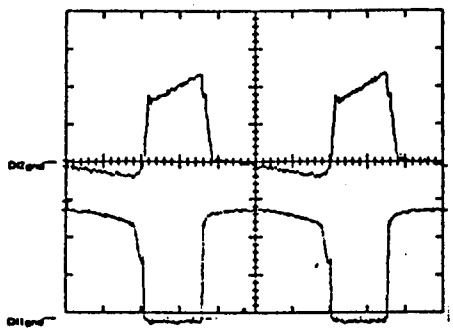

Figure 11a: (200kHz)
CH1: Drain voltage (200V/div)
CH2: Primary current (0.5A/div)
Time:1us/div

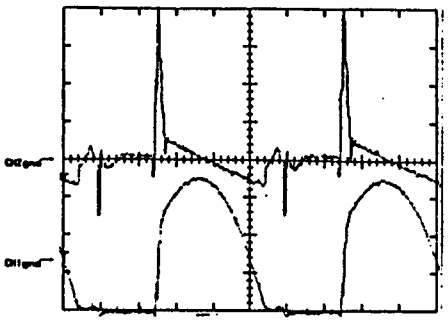

Figure 11b: (200kHz)
CH1: Clamp cap ripple voltage(20V/div)
CH2: Clamp cap current (0.2A/div)
Time:1us/div

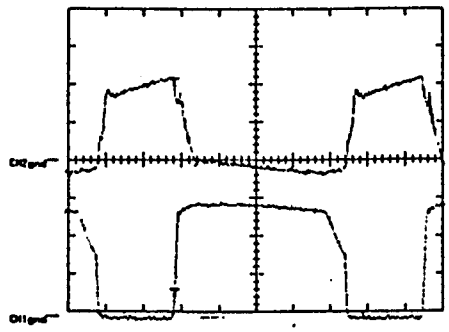

Figure 11c: (300kHz)
CH1: Drain voltage (200V/div)
CH2: Primary current (0.5A/div)
Time:500ns/div

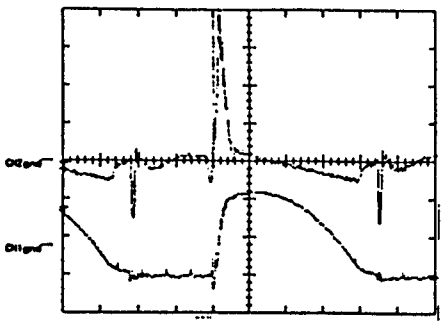

Figure 11d: (300kHz)
CH1: Clamp voltage ripple(20V/div)
CH2: Clamp current (0.2A/div)
Time:500ns/div

Fig. 12 show the waveforms of the clamp capacitor ripple voltage, for different specified values and for 200kHz and 300kHz of switching frequency.

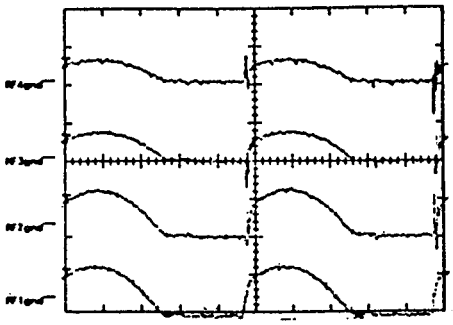

Figure 12a: (200kHz)
REF1:50V/div (2.7nF)
REF2:20V/div (6.8nF)
REF3:20V/div (10nF)
REF4:20V/div (15nF)
Time: 1us/div

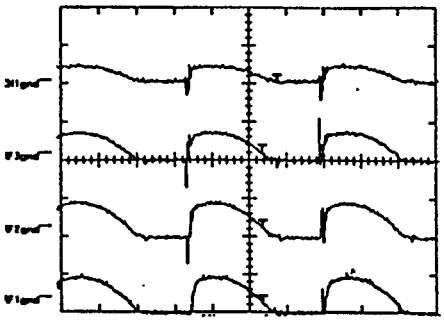

Figure 12b:(300kHz)
REF1:50V/div (2.7nF)
REF2:20V/div (6.8nF)
REF3:20V/div (10nF)
REF4:20V/div (15nF)
Time: 1us/div

These ripple voltage results agree with the calculations of formulas (4) and (5).

CONCLUSIONS

The active clamp is gaining popularity to power shifter), and L4990 (advanced PWM controller), in kit with an supply designers, due to the benefits described in this paper.
The use of the two IC's, L6380 (high voltage level inexpensive N-Channel power MOS, makes this approach more attractive and cost effective for off-line applications.

References:

1) B. Andreycak, "Active Clamp and Reset Technique Enhances Forward Converter Performance", Unitrode Power Supply Design Seminar SEM-1000, 1994.

2) B. Carsten, "Design Technique for Transformer Active Reset Circuits at High Frequency and Power Levels", High Frequency Power Conversion Proceedings, 1990 pp.235-246.

3) D. Dalal - L. Wofford, "Novel Control IC for Single-Ended Active Clamp Converters" High Frequency Power Conversion Proceedings, 1995 pp.136-146.